Kontron User's Guide

X-board™ <GP8>

Document Revision 1.12

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1 User Information

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Technicians and engineers from Kontron Embedded Modules GmbH and/or its subsidiaries are available for technical support. We are committed to making our product easy to use and will help you use our products in your systems.

Before contacting Kontron Embedded Modules GmbH technical support, please consult our Web site at http://www.kontron-emea.com/emd for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone or email.

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2 INTRODUCTION

2.1 X-board™ Benefits

The X-board™ modules of Kontron Embedded Modules GmbH are very compact (49mm x 68mm x 6mm) and highly integrated computers. All X-board™ modules have a standardized form factor and a standardized connector (DDR-SODIMM Memory Connector) that carries a specified set of signals. This standardization allows designers to create a single system “baseboard” which can accept a variety of present and future X-board™ modules.

X-board™ modules include common personal computer (PC) peripheral functions such as serial ports, Ethernet, IDE, USB, etc.

The baseboard designer can optimize exactly how each of these functions is physically implemented. Connectors can be placed precisely where they are needed for the application, on a baseboard designed to optimally fit the system configuration and layout.

Legacy devices are omitted to reach a maximum in compactness and size.

Peripheral PCI devices can be implemented directly on the baseboard rather than on mechanically unwieldy expansion cards. The ability to build a system on a single baseboard, using the computer as one “plug in” component, simplifies packaging, eliminates cabling, and significantly reduces system-level cost.

A single baseboard design may be used with a range of X-board™ modules. This flexibility can be used to differentiate products at various price/performance points, or to design “future proof” systems that have a built-in upgrade path. The modularity of an X-board™ solution also insures against obsolescence as computer technology continues to evolve. A properly designed X-board™ baseboard can be used with several successive generations of X-board™ modules.

An X-board™ baseboard design thus has many of the advantages of a custom computer board design, but delivers better obsolescence protection, greatly reduced engineering effort, and faster time to market.

2.2 X-board™ Documentation

This manual is intended as one of three principal references for an X-board™ design.

- The X-board™ specification defines the X-board™ module form factor, pinout and signals. It is suggested that this be read first.
- The design guide is intended as a general guide for baseboard design, with a focus on maximum flexibility in order to accommodate a wide range of X-board™ modules.
- Finally, the technical manuals for specific X-board™ modules document the specifications and features of each individual X-board™ module.

3 Specifications

3.1 Functional Specifications

- Processor: Intel® XScale® 80219 General Purpose PCI Processor
- Core Speed: 400/600MHz processor clock
- Cache: 32KB integrated instruction and data cache
- Companion Chipset: Silicon Motion SM501 with 8MB Internal SDRAM
- Onboard DDR-SDRAM with 64/128MB and Flash Memory with 8/16/32/(on request) 64MB
- Two Serial Ports (COM1 and COM2)
  - Transistor-to-transistor (TTL) signals
- Intelligent Drive Electronics (IDE):
  - Programmed Input/Output (PIO) mode supported
- Universal Serial Bus (USB)
  - Two USB 2.0(Full Speed) Host ports
  - One USB 2.0(Full Speed) Client port (device)
- Peripheral Component Interconnect Bus (PCI, Version 2.1 compliant)
- Onboard Ethernet: Davicom DM9102A PCI single chip
  - 10BASE-T/100BASE-T LAN
  - Fast Ethernet NIC controller
- Onboard TFT and STN display driver integrated in SM501
  - Resolution up to 1024x768 pixels
- Onboard CRT integrated in SM501
  - Resolution up to 1280x1024 pixels
- Audio: Integrated AC'97 Interface on SM501
  - AC'97 Rev 2.0 Interface to connect an AC'97 codec
- Several GPIO's
  - 16-bit Video Capture Port or 8 GPIOs
  - 1 x GP Chip Select
- Watchdog timer (WDT)
- JTAG interface for easy debugging
- Wake on LAN, Wake on RTC support (both from Soft-OFF State).

3.2 Mechanical Specifications

3.2.1 Dimensions

- 49.0 mm x 68.0 mm
- Height approx. 6 mm

3.3 Electrical Specifications

3.3.1 Supply Voltage

- 3.3V DC +/- 5%

3.3.2 Supply Voltage Ripple

- 100 mV peak to peak 0 - 20 MHz

3.3.3 Supply Current

- approx. 700mA @ 3.3V
- TBD accurate measurement

It was measured with a 600MHz board/64MB RAM connected in a backplane without additional power consuming components.

3.4 Environmental Specifications

3.4.1 Temperature

- Operating: 0 to +70°C
- Non operating: -10 to +85°C

Note: *The maximum operating temperature is the maximum measurable temperature on any spot on a module's surface. You must maintain the temperature according to the above specification.*

3.4.2 Humidity

- Operating: 10% to 90% (non condensing)
- Non operating: 5% to 95% (non condensing)

4 CPU, COMPANION and Bridge CHIPset

4.1 Processor Intel® XScale™ 80219 General Purpose PCI Processor

Intel® XScale™ 80219 General Purpose PCI Processor application processor is a 32-bit RISC based processor incorporating Intel's XScale™ Micro architecture based on the ARM* V5T architecture.

- ARM* Architecture Version 5T ISA compliant
- ARM* V5T Instruction Set
- ARM* V5E DSP Enhanced Instructions
- 32KB Instruction Cache / 32kB Data Cache / 2 KB "mini" Data Cache, Extensive Data Buffering
- PCI Bus Interface. PCI Local Bus Specification, Rev 2.2 compliant.
- PC200 DDR-SDRAM interface for maximum efficiency
- Low power modes
- I2C Interface
- DMA Controller

4.2 Companion Chipset Silicon Motion SM501

The SM501 is a Mobile Multimedia Companion Chip (MMCC™) device which connects to the PCI Bus. It provides video and 2D capability. It supports a wide variety of I/O, including analog RGB and digital LCD Panel interfaces, USB, UART, AC97 and I2C. There are additional GPIO bits that can be used to interface to external devices as well or to be used as an 8-bit Video Capture Port.

This Video Capture Port can be used, for example, to interconnect to a MPEG-4 video decoder, such as Sigma EM8470. Interconnection example is shown later on.

It runs with its own Local SDRAM Memory, not impacting the whole system performance like in UMA (Unified Memory Architecture) Systems.

5 System and flash memory

5.1 DDR-SDRAM

The X-board<GP8> uses onboard Double Data Rate Synchronous Dynamic Random Access Memory (SDRAM) sizes of 64 or 128MB.

5.2 Flash

The X-board<GP8> is optionally equipped with 32 or 64MB Flash memory.

6 Interfaces

6.1 PCI Bus

The implementation of this subsystem complies with the *X-board™* Specification. Implementation information is provided in the *X-board™ Design Guide*. Refer to the documentation for additional information.

6.2 LPC Bus

LPC bus is not supported on the X-board<GP8>
The signals are used as GPIOs/ZV Port. See Pinout (Appendix D) for more information.

6.3 IDE Port (PIO Mode)

The implementation of this subsystem complies only in PIO Mode with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.4 Serial ATA Signals

Serial ATA is not supported on the X-board<GP8>

6.5 Serial Ports (COM1 and COM2)

The implementation of the serial-communication interface is restricted. COM1 supports all UART signals RXD, TXD, DTR#, CTS#, RTS#, DCD#, RI, DSR#, COM2 includes RXD, TXD, RTS# and CTS#. Implementation information is provided in the *X-board™ Design Guide*. Refer to the documentation for additional information.

6.6 USB

Two EHCI-type USB host controllers and one OHCI-type device controller are supported on the X-board<GP8> module. The USB controllers comply with Version 2.0 up to Full Speed of the USB standard. The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.7 Ethernet

The Davicom DM9102ATE/DE is a cost-effective 10BASE-T/100BASE-TX LAN solution. It is designed for low-power use and high-performance processes.

Configuration

The Ethernet interface is a PCI device. The operating system will automatically configure this controller.

6.8 AC'97 Codec Interface

The sound function on the *X-board<GP8>* board comes from the AC'97 interface of the Silicon Motion SM501. An external Codec must be connected on the baseboard to use the audio functions. Please look at the implementation information provided in the *X-board™ Design Guide*.

Configuration

The audio controller is an internal interface of Silicon Motion SM501. The operating system will allocate required system resources during startup.

6.9 VGA Output

The SM501 includes the display subsystem:
The LCD Controller supports both passive (DSTN) and active (TFT) flat-panel displays with a maximum supported resolution of 1024x768x18-bit/pixel.
The analog RGB block contains a 24-bit DAC (RGB 8:8:8) to drive an external analog RGB interface. The 200MHz DAC will easily support the maximum resolution of 1280 x 1024.

6.10 Digital Flat Panel Interface

The *X-board<GP8>* supports the Intelligent LCD Interface **(referred to as either JIDI or JILI-d)**. It provides the possibility to store controller specific panel configuration data in an external EEPROM. Please contact Kontron Embedded Modules Technical Support for more information.

6.11 Television Output

The *X-board<GP8>* does not support television output.

6.12 SMB/I2C BUS

The X-board<GP8> provides only the I²C bus on that interface. The Silicon Motion SM501 internal I²C controller is not used.
A second I²C bus is implemented onboard for JILI/JILI-d devices

6.13 Power Control

6.13.1 Power Good / Reset Input

The *X-board<GP8>* provides an external input for a power good signal or a manual reset pushbutton. The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.14 Power Management

6.14.1 ATX PS Control

The X-board<GP8> can control the main power output of an ATX-style power supply. The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.15 Watchdog Timer

This feature is implemented in the Intel 80219. It could be eventually be implemented on Silicon Motion SM501. The Watchdog can be configured in the customer application to start after a set amount of time following power-on boot. The application software should strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

Configuration

The watchdog can be programmed using the Standard JIDA32 Library API in a board and OS independent manner. Please refer to the JIDA32 Library API documentation. For hardware low level programming please refer to the Intel® XScale™ 80219 manual.

6.16 PCI

An onboard PCI Arbiter is implemented to provide PCI Bus Master capabilities. Up to two external PCI Bus Masters are supported.
The implementation of this subsystem complies with the *X-board™ Specification*. Implementation information is provided in the *X-board™ Design Guide*. Refer to those documents for additional information.

6.17 Keyboard / Mouse usage

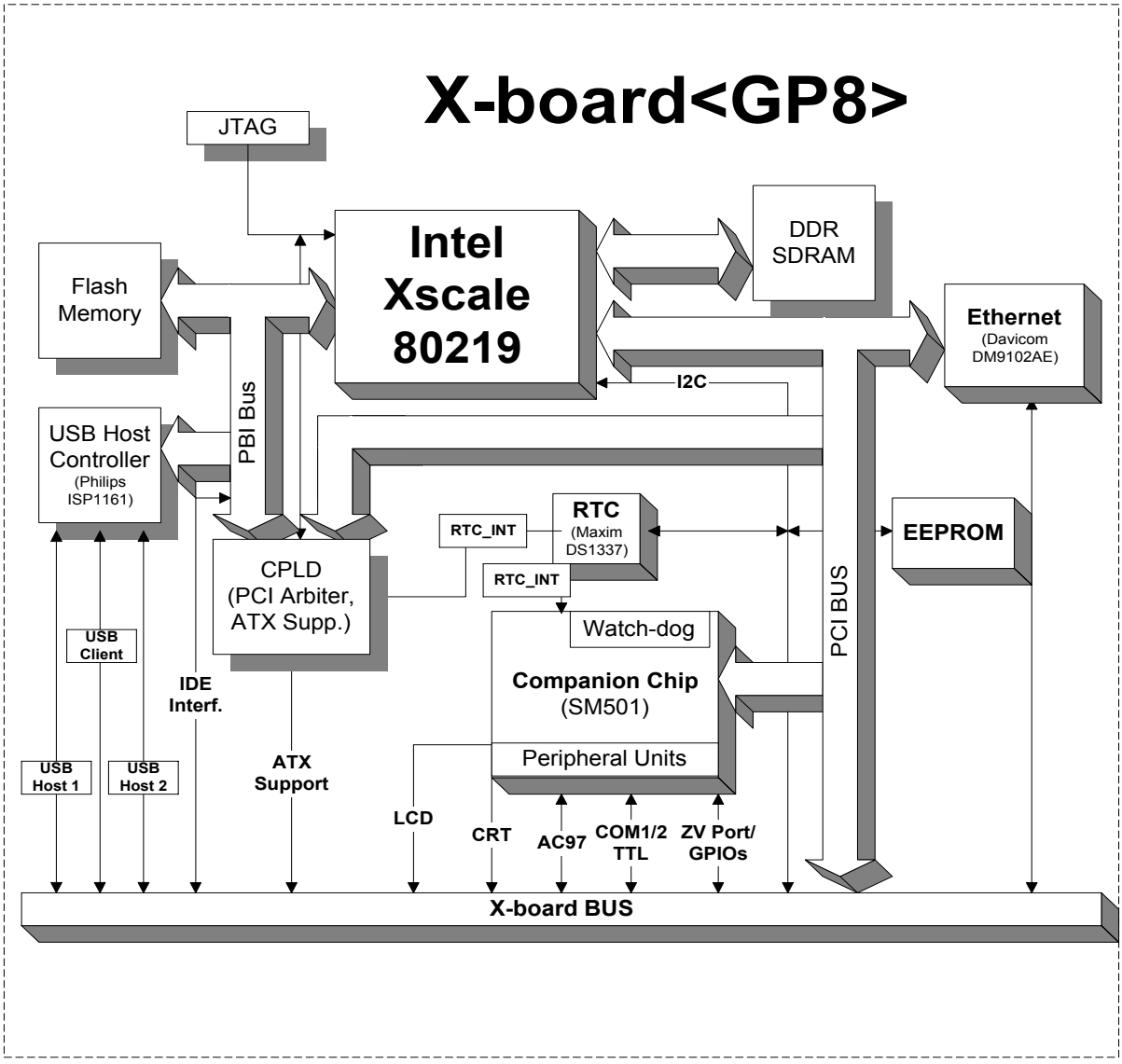
You can either use a USB mouse and keyboard.

6.18 RTC

An onboard I²C bus RTC is supported on X-board<GP8> modules.
This RTC can generate two different Interrupts (based on internal alarms).

RTC_INTA: connected to CPLD to generate a WAKE on RTC Event.
RTC_INTB: connected to SM501 to generate a general purpose Interrupt.

7 Appendix a: block diagram



8 Appendix B: System Resources

8.1 Memory Area

Address Range [hex]	Resource Size	Function	Note
0000 0000 – 7FFF FFFF	2 GB	ATU Outbound Direct Window	
8000 0000 – 900F FFFF	257 MB	ATU Outbound Translate Windows	
A000 0000 – BFFF FFFF	512 MB	SDRAM	Usable space depends on assembled memory size
F000 0000 – F200 0000	32 MB	Flash	Usable space depends on assembled memory size
FE80 0000 – FE80 0FFF	4 kB	GFE	
FE81 0000 – FE81 0FFF	4 kB	USB Host Controller ATX Power Down	Write access to not word aligned registers powers the system down
FE8E 0000 – FE8E FFFF	64 kB	IDE Buffer Enable	
FE8E 0000 – FE8E 0FFF	4 kB	IDE	Overlaps with IDE Buffer Enable
FE8E 1000 – FE8E 1FFF	4 kB	IDE extended	Overlaps with IDE Buffer Enable
FFF0 0000 – FFFF FFFF	1 MB	80219 Memory mapped Registers	

8.2 Flash Memory Layout

Address Range [hex]	Resource Size	Function	Note
F000 0000 – F003 FFFF	256 kB	RedBoot boot loader	Do not overwrite this space!
F004 0000 – F007 FFFF	256 kB	WinCE boot loader	Only usable if no WinCE bootloader is needed!
F008 0000 – F1FB FFFF	31 480 kB	Freely usable space	
F1FC 0000 – F1FC FFFF	4 kB	RedBoot boot loader configuration	Do not overwrite this space!
F1FE 0000 – F1FF FFFF	128 kB	FIS directory	Do not overwrite this space!

Note: *The flash memory layout above is only valid for the 32 MB flash version of the X-board<GP8> and may also change with newer boot loader versions. To be sure which space is really available, you can get the actual layout by invoking the "fis list" command in the boot loader shell.*

8.3 Peripheral Component Interconnect (PCI) Devices

PCI Device	PCI Interrupt	Comment
SM501	INTA	80219 XINT0, Use REQ0/GNT0 pair
IDE	INTA	Handled via interrupt-capable SM501 GPIO
Ethernet	INTB	80219 XINT1, Use REQ1/GNT1 pair
USB Host Controller	INTB	80219 XINT1

You can use only REQ2/GNT2 and REQ3/GNT3 pairs for external PCI devices. In the *X-board™ Design Guide* you find additional information about how to expand these pairs by using certain devices on the backplane

Only INTC and INTD are externally available. INTD may be shared with IDE interrupt in future revisions.

9 Appendix C: Bootloader

9.1 Boot Loader

The boot loader is the low-level code that configures the X-board<GP8> and loads the OS image. On the X-board<GP8> we use a modified version of the RedBoot bootloader available at:

http://sources.redhat.com/redboot/

There is also an X-board<GP8> specific manual for the RedBoot boot loader included in the Board Support Package.

Note: *Never attempt to change the boot loader unless you have a working JTAG programmer and cable. If there's a problem with the boot loader code you will no longer be able to download new code and JTAG is the only means to revive the board.*

9.2 Boot Loader Shell

During the boot process, the boot loader displays status information and a shell is available over the COM1 serial port. You can view this information and use the shell with a RS232 terminal program. For a Windows host you can use the the Microsoft HyperTerminal terminal emulation or Teraterm for example. For a Linux host minicom would be a good choice. Use a null modem cable to connect the COM1 port of the X-board<GP8> to your development workstation. This is the bottom connector on the Kontron X-board Eval Backplane.

To configure HyperTerminal:

- From the Windows Start menu, choose All Programs and then choose Accessories.
- Choose Communications and then choose HyperTerminal.
- In the Connection Description dialog box, in the Name box, type a name for the connection to your X-board<GP8>.
- From the Icon list, choose an icon to represent your connection and then choose OK.
- In the Connect To dialog box, in the Connect using box, choose the communications (COM) port on the development workstation through which you want to receive messages from the X-board<GP8>.
- The COM port that you choose must be the COM port on the development workstation to which you attached the null modem cable.
- Choose OK.
- In the COM<Port Number> Properties dialog box, modify the settings for your connection so that the settings are correct for your BSP.

The following table shows the correct settings:

Bits per second	Data bits	Parity	Stop bits	Flow control
38400	8	None	1	None

10 Appendix d: X-board connector pinouts

Pin number	Signal	Signal type	Pin number	Signal	Signal type
1	VP_CLK	I_1	2	PWRGOOD_IN	I_2
3	N.C.		4	V_BAT	P
5	Codec_SDATA_OUT	O_1	6	VP_HREF	I_1
7	Codec_SDATA_IN	I_1	8	GND	P
9	Codec_BIT_CLK	I_I	10	R	O_4
11	Codec_SYNC	O_1	12	G	O_4
13	Codec_RESET#	O_1	14	B	O_4
15	GND	P	16	GND	P
17	Lan TX-	O_2	18	CRT_HSYNC	O_4
19	Lan TX+	O_2	20	CRT_VSYNC	O_4
21	Lan RX-	O_2	22	V33	P
23	Lan RX+	O_2	24	R5	O_1
25	Lan LNLED#	O_3	26	R4	O_1
27	Lan LNKLED#	O_3	28	R3	O_1
29	V33	P	30	R2	O_1
31	USB[1]+	O_{USB}	32	R1	O_1
33	USB[1]-	O_{USB}	34	R0	O_1
35	Overcurrent#	I_3	36	GND	P
37	USB[2]+	O_{USB}	38	G5	O_1
39	USB[2]-	O_{USB}	40	G4	O_1
41	GND	P	42	G3	O_1
43	DCD1#	I_1	44	G2	O_1
45	DSR1#	I_1	46	G1	O_1
47	RXD1	I_1	48	G0	O_1
49	RTS1#	O_1	50	V33	P
51	TXD1	O_4	52	B5	O_1
53	CTS1#	I_1	54	B4	O_1
55	DTR1#	O_1	56	B3	O_1
57	RI1#	I_1	58	B2	O_1
59	V33	P	60	B1	O_1
61	RXD2	I_1	62	B0	O_1
63	RTS2#	O_1	64	GND	P
65	TXD2	O_4	66	HSYNC	O_1
67	CTS2#	I_1	68	VSYNC	O_1
69	V33	P	70	DE	O_1
71	VP_VSYNC	I_1	72	SCLK	O_{PC}
73	GND	P	74	GND	P
75	ZV(0)	I/0	76	BIASON	I/0
77	ZV(1)	I/0	78	DIGON	O_1
79	ZV(2)	I/0	80	V33	P
81	ZV(3)	I/0	82	V33-Standby	P
83	GND	P	84	Power Button#	I_1
85	AD[00]	I/0	86	Resume/Reset#	O_1
87	AD[01]	I/0	88	ZV(7)	I/0
89	AD[02]	I/0	90	N.C.	
91	AD[03]	I/0	92	GPIO(11)	O_4
93	AD[04]	I/0	94	PS_ON#	O_5

Pin number	Signal	Signal type	Pin number	Signal	Signal type
95	AD[05]	I/O	96	N.C.	
97	AD[06]	I/O	98	GND	
99	AD[07]	I/O	100	ZV(15)	I_1
101	AD[08]	I/O	102	ZV(14)	I_1
103	C/BE[0]#	I/O	104	ZV(13)	I_1
105	AD[09]	I/O	106	ZV(12)	I_1
107	AD[10]	I/O	108	ZV(11)	I_1
109	AD[11]	I/O	110	ZV(10)	I_1
111	AD[12]	I/O	112	ZV(9)	I_1
113	AD[13]	I/O	114	ZV(8)	I_1
115	AD[14]	I/O	116	V33	P
117	C/BE[1]#	I/O	118	USB[3]+ (USB Client)	O_{USB}
119	AD[15]	I/O	120	USB[3]- (USB Client)	O_{USB}
121	LOCK#	I/O_1	122	V33	P
123	PERR#	I/O_1	124	I2C_CLK	I/O_2
125	DEVSEL#	I/O_1	126	I2C_DAT	I/O_2
127	SERR#	I/O_1	128	GND	P
129	STOP#	I/O_1	130	IDE_DASP	I/O_3
131	CLKRUN#	-	132	IDE_PDIAG	I/O_3
133	TRDY#	I/O_1	134	V33	P
135	IRDY#	I/O_1	136	IDE_CS3#	I/O_1
137	FRAME#	I/O	138	IDE_CS1#	I/O_1
139	AD[16]	I/O	140	IDE_A2	I/O_1
141	C/BE[2]#	I/O	142	IDE_A0	I/O_1
143	AD[17]	I/O	144	IDE_A1	I/O_1
145	PAR	I/O_1	146	GND	P
147	AD[18]	I/O	148	IDE_INTRQ	I_8
149	AD[19]	I/O	150	IDE_AK#	I/O_1
151	AD[20]	I/O	152	N.C.	
153	AD[21]	I/O	154	IDE_IOR#	I/O_1
155	AD[22]	I/O	156	IDE_IOW#	I/O_1
157	AD[23]	I/O	158	N.C.	
159	C/BE[3]#	I/O	160	GND	P
161	AD[24]	I/O	162	IDE_D0	I/O_1
163	AD[25]	I/O	164	IDE_D1	I/O_1
165	AD[26]	I/O	166	IDE_D2	I/O_1
167	AD[27]	I/O	168	IDE_D3	I/O_1
169	AD[28]	I/O	170	IDE_D4	I/O_1
171	AD[29]	I/O	172	V33	P
173	AD[30]	I/O	174	IDE_D5	I/O_1
175	N.C.		176	IDE_D6	I/O_1
177	AD[31]	I/O	178	IDE_D7	I/O_1
179	REQ3#	I_6	180	IDE_D8	I/O_1
181	GNT3#	I_5	182	IDE_D9	I/O_1
183	REQ2#	I_6	184	IDE_D10	I/O_1
185	GNT2#	I_5	186	GND	P
187	RST#	O_1	188	IDE_D11	I/O_1
189	CLK1	O_1	190	IDE_D12	I/O_1
191	ZV(4)	I/O	192	IDE_D13	I/O_1
193	ZV(5)	I/O	194	IDE_D14	I/O_1

Pin number	Signal	Signal type	Pin number	Signal	Signal type
195	ZV(6)	I/0	196	IDE_D15	I/O_1
197	INTC#	I_6	198	HDRST#	O_1
199	INTD#	I_6	200	GND	P

Note: ** If the LPC interface is not used on the customer's Backplane, the Signals LAD[0..3] and LDRQ# have to be connected together and pulled-up to 3.3V with an 15kΩ resistor.*

- I1 Input, TTL compatible.
- I_2 Input, low active with open collector/button.
- I_3 Input, TTL compatible with Schmitt-Trigger. Internally pulled up (10kΩ) .
- I_4 Input, TTL compatible. Internally pulled up (10kΩ).
- I_5 Input, TTL compatible. Internally pulled down (4,7kΩ).
- I_6 Input, TTL compatible. Internally pulled up (2,7KΩ).
- O_1 Output 3,3V (3,14V-3,46V), source 2mA, sink 5mA.
- O_2 Output, differential pair.
- O_3 Output, open collector. 5V tolerant.
- O_4 Output. Do not pull up or down externally!
- O_{USB} Output. Internally pulled down (15kΩ).
- I/O Input/Output.
- I/O_1 Input/Output. Internally pulled up (2,7kΩ).
- I/O_2 Input/Output. Internally pulled up (10kΩ).
- P Power Input.

10.1 General purpose I/O's (GPIO's)

Pin no. (X-board)	GPIO in X-board Spec.	GPIO Signal used on X-Board <GP8>	Description
1	BUZZER	VP_CLK	Video Port Clock
6	Composite	VP_HREF	Video Port Horizontal Reference
10	GPIO[8]	R	CRT Red Output
12	GPIO[12]	G	CRT Green Output
14	GPIO[13]	B	CRT Blue Output
18	GPIO[10]	CRT_HSYNC	CRT Horizontal Sync
20	GPIO[11]	CRT_VSYNC	CRT Vertical Sync
71	GPIO[1]	VP_VSYNC	Video Port Vertical Sync
75	MMC_SMD	ZV(0)*	Video Port bit 0 / GPIO16 from SM501
77	MMD_DAT	ZV(1)*	Video Port bit 1 / GPIO17 from SM501
79	MMC_CLK	ZV(2)*	Video Port bit 2 / GPIO18
81	GPIO[2]	ZV(3)*	Video Port bit 3 / GPIO19 from SM501
88	GPIO[4]	ZV(7)*	Video Port bit 7 / GPIO23 from SM501

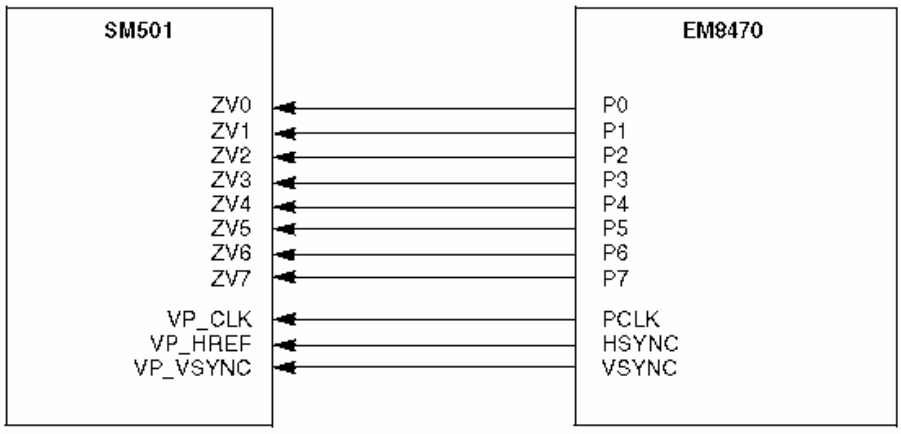
92	GPE1#	GPIO[11]	GPIO11 from SM501
191	GPIO[5]	ZV(4)*	Video Port bit 4 / GPIO20 from SM501
193	GPIO[6]	ZV(5)*	Video Port bit 5 / GPIO21 from SM501
195	GPIO[7]	ZV(6)*	Video Port bit 6 / GPIO22 from SM501
100	LAD[3]	ZV(15)*	Video Port bit 15 / GPIO63 from SM501
102	LAD[2]	ZV(14)*	Video Port bit 14 / GPIO62 from SM501
104	LAD[1]	ZV(13)*	Video Port bit 13 / GPIO61 from SM501
106	LAD[0]	ZV(12)*	Video Port bit 12 / GPIO60 from SM501
108	LDRQ#	ZV(11)*	Video Port bit 11/ GPIO59 from SM501
110	LFRAME#	ZV(10)*	Video Port bit 10 / GPIO58 from SM501
112	LPCPD#	ZV(9)*	Video Port bit 9 / GPIO57 from SM501
114	SERIRQ#	ZV(8)*	Video Port bit 8 / GPIO56 from SM501

Note: ** ZV Port Signals can be defined as standard GPIOs (see SM501 Manual for more information).*

10.2 Zoom Video Capture Port

The SM501 Zoom Video Port (ZV Port) can interface with video decoders, such as NTSC/PAL decoders, MPEG-2 decoders, and JPEG codecs. The ZV Port supports resolutions up to 1280x1024. It directly accepts digitized RGB or YUV signals, and does not accept analog signals.

The next figure shows and example of an 8-bit interconnection between the SM501 ZV Port and the Sigma Designs EM8470 MPEG-4 Decoder.



For more information on Capture Port interconnection and use refer to Silicon Motion SM501 Datasheet.

10.3 LCD Panel Pinout Table

Pin no. (X-board)	18-bit Active TFT panel	12-bit Active TFT panel	9-bit Active TFT panel	12-bit Passive CSTN panel	8-bit Passive CSTN panel
62	B0				
60	B1				
58	B2	B0			
56	B3	B1	B0		
54	B4	B2	B1		
52	B5	B3	B2		
48	G0			D0	D0
46	G1			D1	D1
44	G2	G0		D2	D2
42	G3	G1	G0	D3	D3
40	G4	G2	G1	D4	D4
38	G5	G3	G2	D5	D5
34	R0			D6	D6
32	R1			D7	D7
30	R2	R0		D8	
28	R3	R1	R0	D9	
26	R4	R2	R1	D10	
24	R5	R3	R2	D11	
72	SCLK	SCLK	SCLK	Pixel_Clock	Pixel_Clock
66	HSYNC	HSYNC	HSYNC	Line_Clock	Line_Clock
68	VSYNC	VSYNC	VSYNC	Frame_Clock	Frame_Clock
70	DE	DE	DE	BIAS	BIAS

10.4 JTAG Interface

The JTAG connector (X2) is mounted by default on the X-board<GP8> for debug purposes.

Two JTAG Devices are placed on Board:

- Intel 80219 (U1)
- Xilinx XC9536XL CPLD (U10, *internal use only*!)

Both devices can be chained together or connected alone on the chain selecting different jumper options.

Both the 80219 and the CPLD are on the chain as default option **BUT** the CPLD is *only for internal use* and should **never be erased or reprogrammed**.

10.4.1 Specification and Pinout of the JTAG connector

4 x 2 pins; 1.27mm (0.050in) pitch; SMD

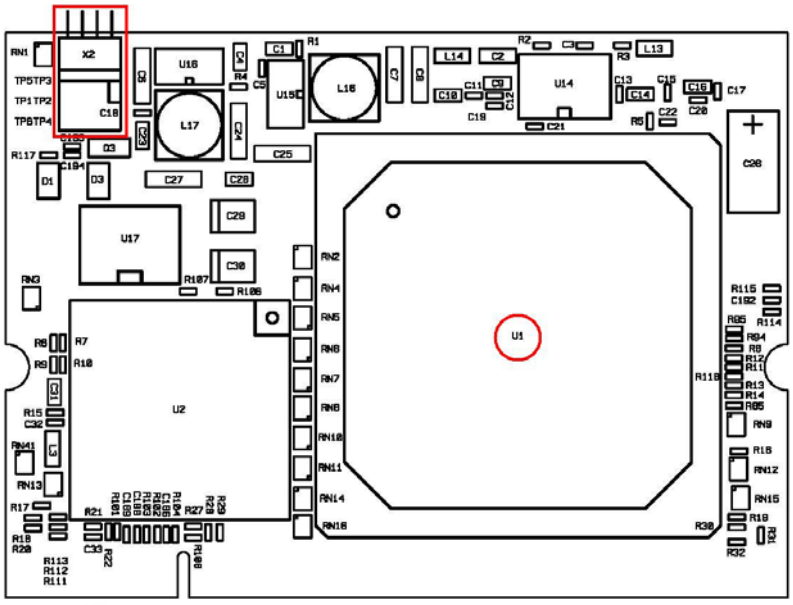
For Example: SAMTEC FTSH-104-02-L-DH

Pin No.	Signal	Description
1	#TRST	Test Interface Reset
2	VCC	Power Supply
3	TDO	Test Data Input
4	#SRST	System Reset
5	TMS	Test Mode Select
6	TDI	Test Data Output
7	TCK	Test Clock
8	GND	Ground

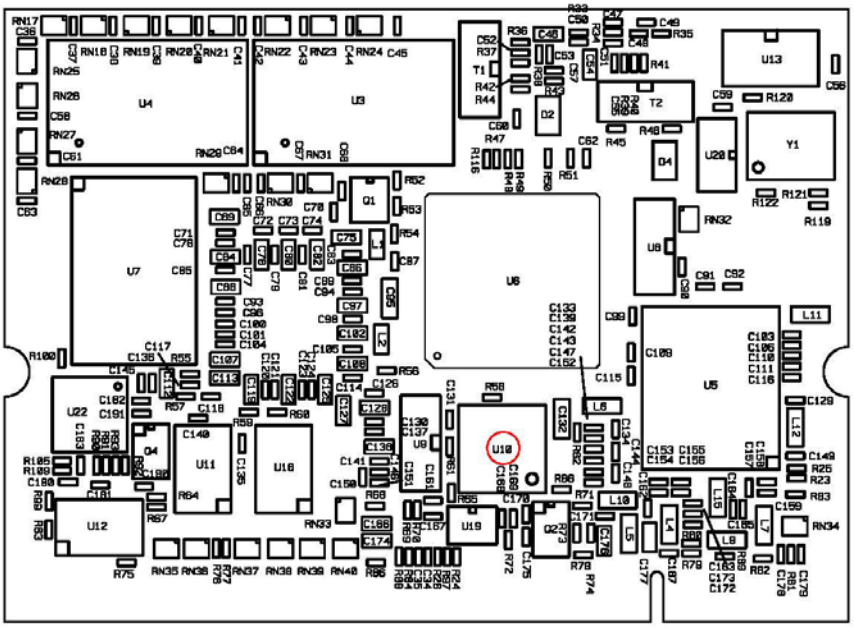
10.4.2 JTAG Chain

No	Device	IR Length
1	80219 (U1)	5
2	CPLD (U10) (Internal use!)	2

10.4.3 Top and Bottom Overlay



Top Overlay



Bottom Overlay

11 Appendix E: JIDA STANDARD

11.1 JIDA Information

To obtain information about boards that follow the JIDA standard refer to the JIDA32 Library API that comes with the BSP. The library itself is also included in the BSP for the X-board<GP8>.

Note: *The X-board<GP8> only supports the JIDA32 Library API functions. The 16-bit legacy JIDA INT15 interface is tied to the x86 architecture and is **NOT** available on this board.*

12 Appendix F: PC Architecture Information

The following sources of information can help you better understand PC architecture.

12.1 Buses

12.1.1 Low Pin Count Bus (LPC)

- Low Pin Count Bus Specification, Aug. 2002, Intel

12.1.2 ISA, Standard PS/2 - Connectors

- AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- AT IBM Technical Reference Vol. 1&2, 1985
- ISA & EISA Theory and Operation, Edward Solari, Annabooks, 1992, ISBN 0929392159
- ISA Bus Specifications and Application Notes, Jan. 30, 1990, Intel
- ISA System Architecture, Third Edition, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- Personal Computer Bus Standard P996, Draft D2.00, Jan. 18, 1990, IEEE Inc
- Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus, Compaq 1989

12.1.3 PCI/104

- Embedded PC 104 Consortium
  The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- PCI SIG
  The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture,* Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

12.2 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8

- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

12.3 Ports

12.3.1 RS-232 Serial

- EIA-232-E standard:
  The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor:
  The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

12.3.2 Serial ATA

- Serial AT Attachment (ATA) Working Group:
  This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.
  We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

12.3.3 USB

- USB Specification:
  USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

12.4 Programming

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook,* Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

13 APPENDIX G: DOCUMENT-REVISION HISTORY

Filename	Date	Edited by	Alteration to preceding revision
XBD7M001.doc	14/07/2005	WEC	Initial Preliminary Release
XBD7M002.doc	21/10/2005	WEC	Added ZV(8:15) Signals to X-Board connector Modified JTAG (Added IR Lengths)
XBD7M003.doc	10/11/2005	WEC	Updated Block diagram Updated GPIO´s table Updated featurelist
XBD7m004.doc	15/12/2005	WEC	Updated functional description list Updated Bootloader Section
XBD7m110.doc	23/08/2006	SAL	Corrected JTAG (TDI/TDO) pin description Renamed Pin92 of X-board to GPIO[11] instead GFE#
XBD7m111.doc	20/11/2006	SAL	Corrected display resolution parameters
XBD7m112.doc	03.07.2007	U. Geisler	Updated to current Kontron Layout